

FIG. 1A
(PRIOR ART)

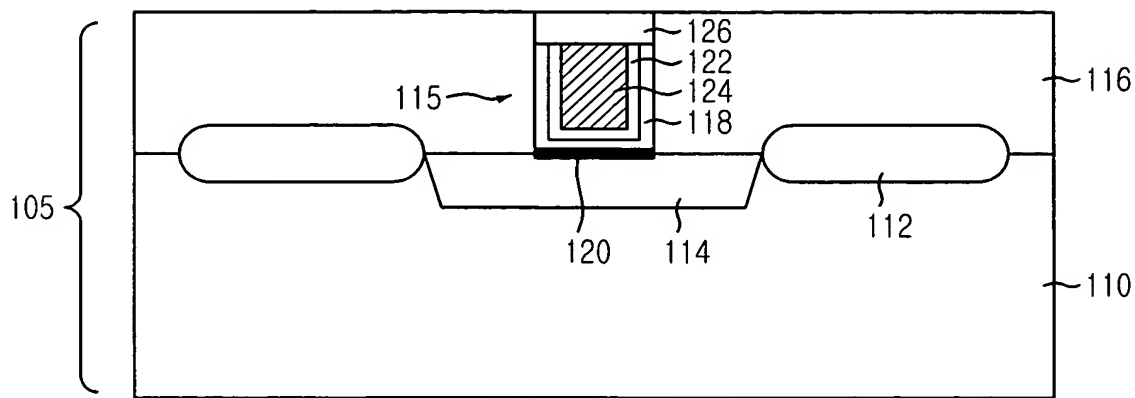


FIG. 1B
(PRIOR ART)

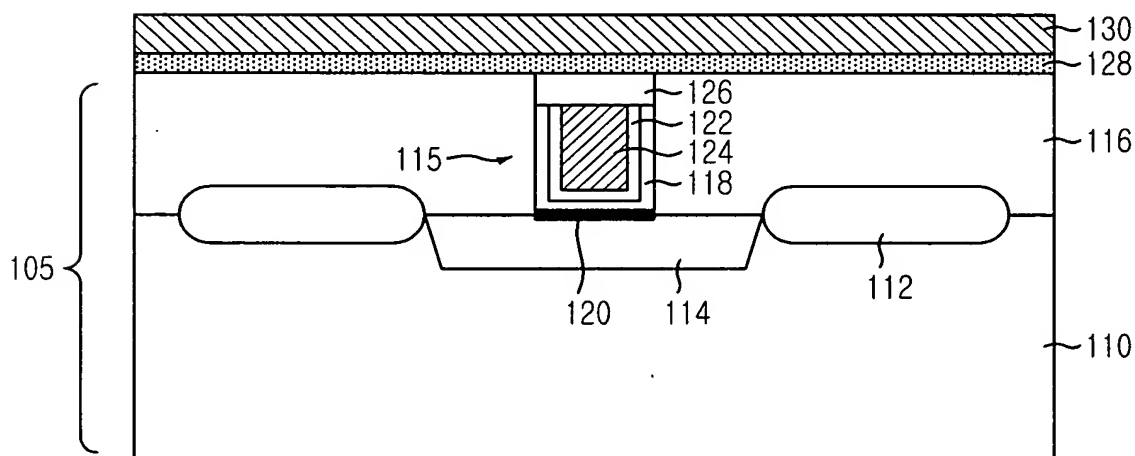


FIG. 1C
(PRIOR ART)

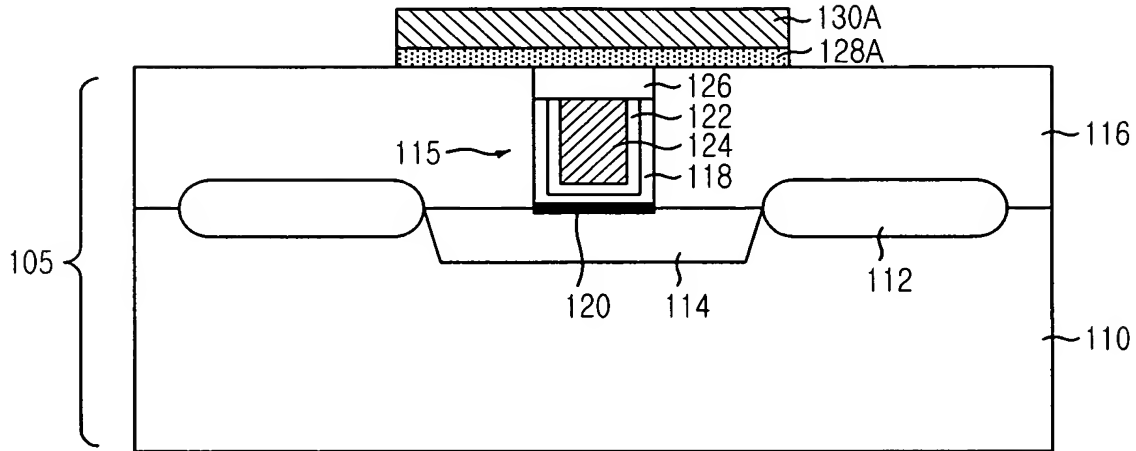


FIG. 1D
(PRIOR ART)

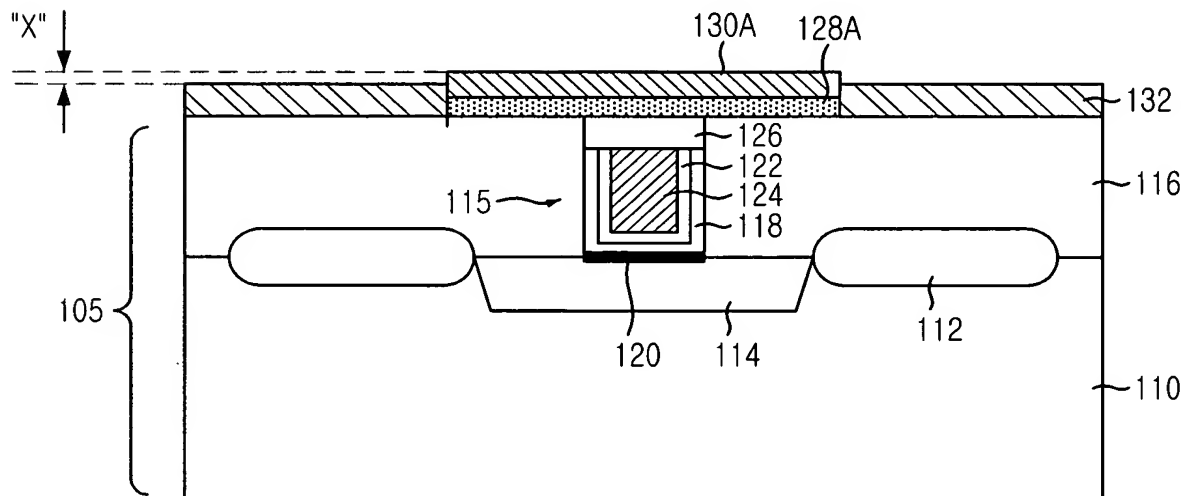


FIG. 1E
(PRIOR ART)

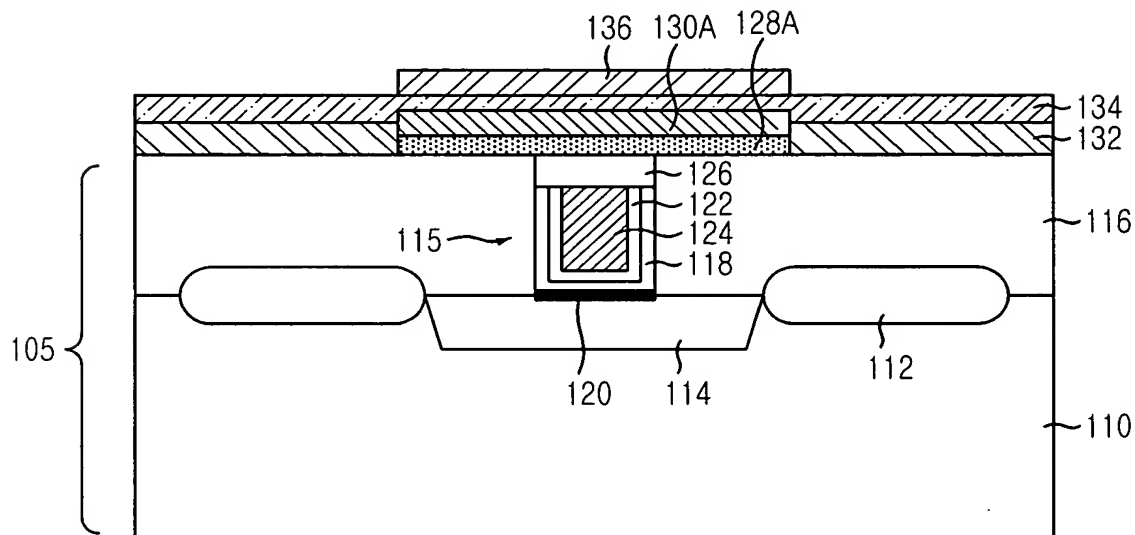


FIG. 2

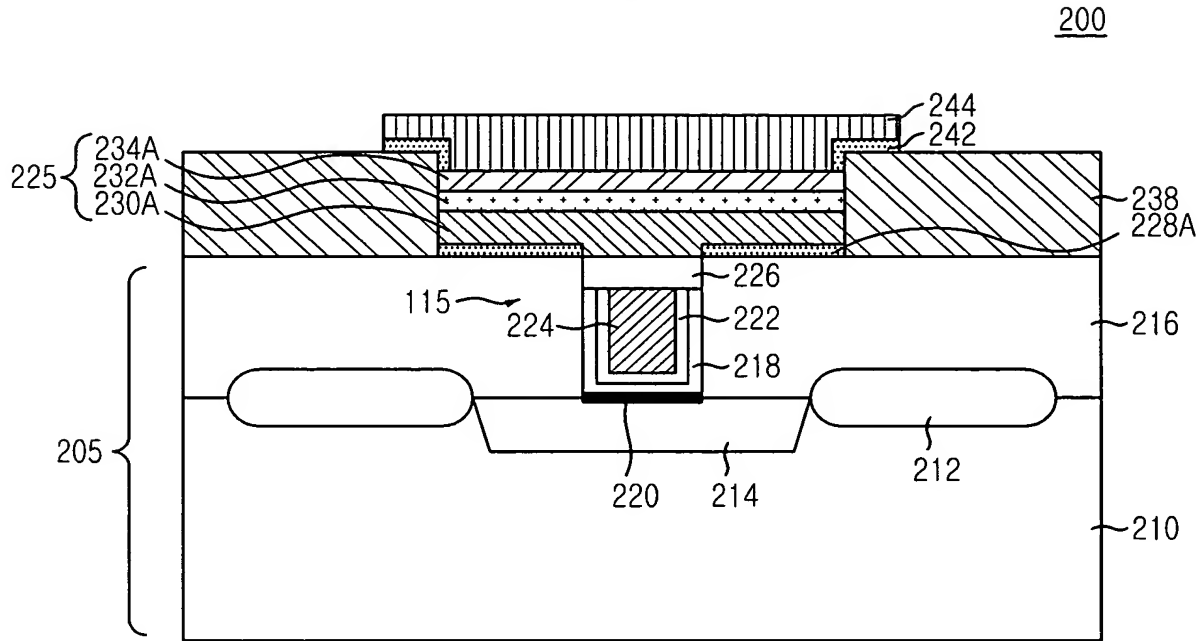


FIG. 3A

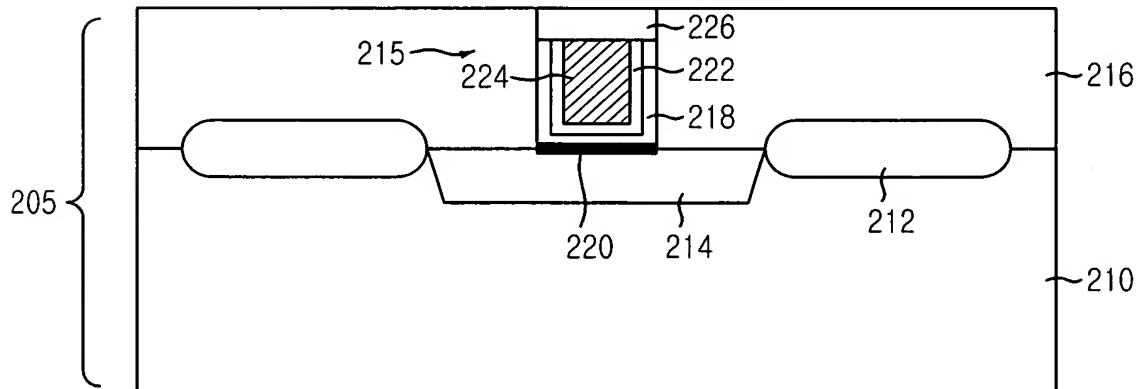


FIG. 3C



[illegible]

A cross-sectional view of a semiconductor device 200. The device features a substrate 210 with a central well region 214. A gate stack 215 is positioned over the well region 214, consisting of a gate dielectric 222, a gate electrode 224, and a gate cap 226. The gate stack 215 is flanked by two side regions 212. The side regions 212 are separated from the gate stack 215 by a trench 220. The side regions 212 are formed in the substrate 210 and are covered by a layer 216. The layer 216 is also present over the gate stack 215 and the trench 220. The layer 216 is composed of a bottom layer 228A and a top layer 230A. The top layer 230A is further divided into a central portion 232A and side portions 234A. The side portions 234A are formed over the side regions 212. The central portion 232A is formed over the gate stack 215. The side portions 234A are formed over the side regions 212 and the central portion 232A. The side portions 234A are formed over the side regions 212 and the central portion 232A. The side portions 234A are formed over the side regions 212 and the central portion 232A.

FIG. 3F

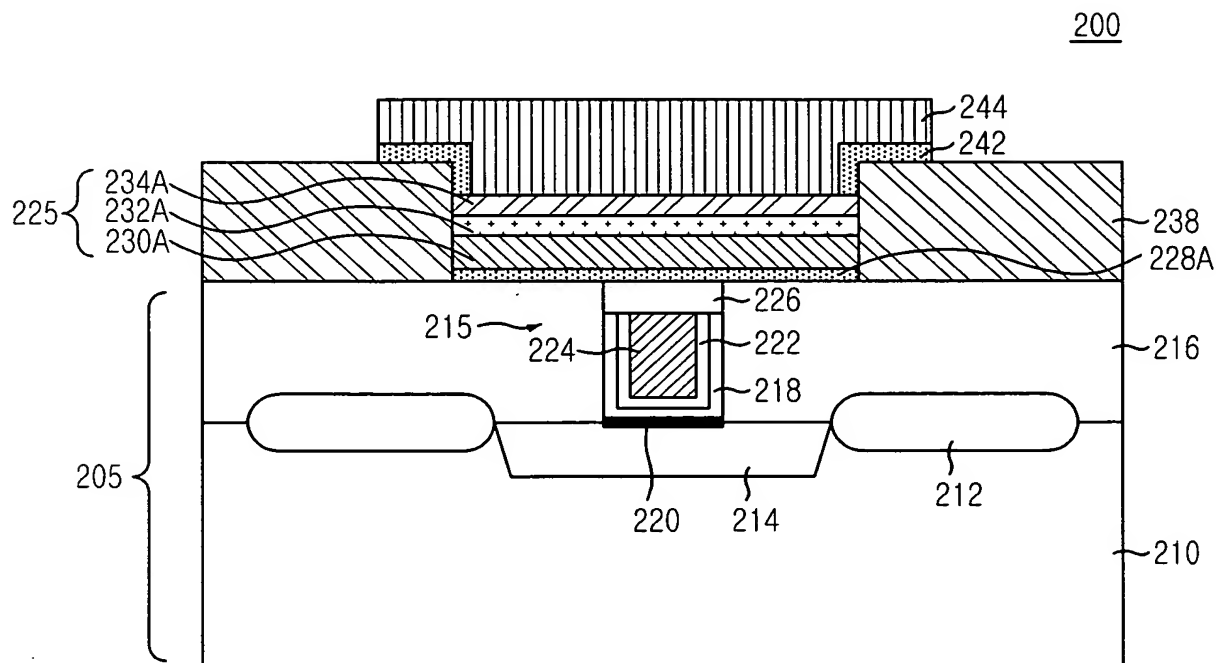


FIG. 4

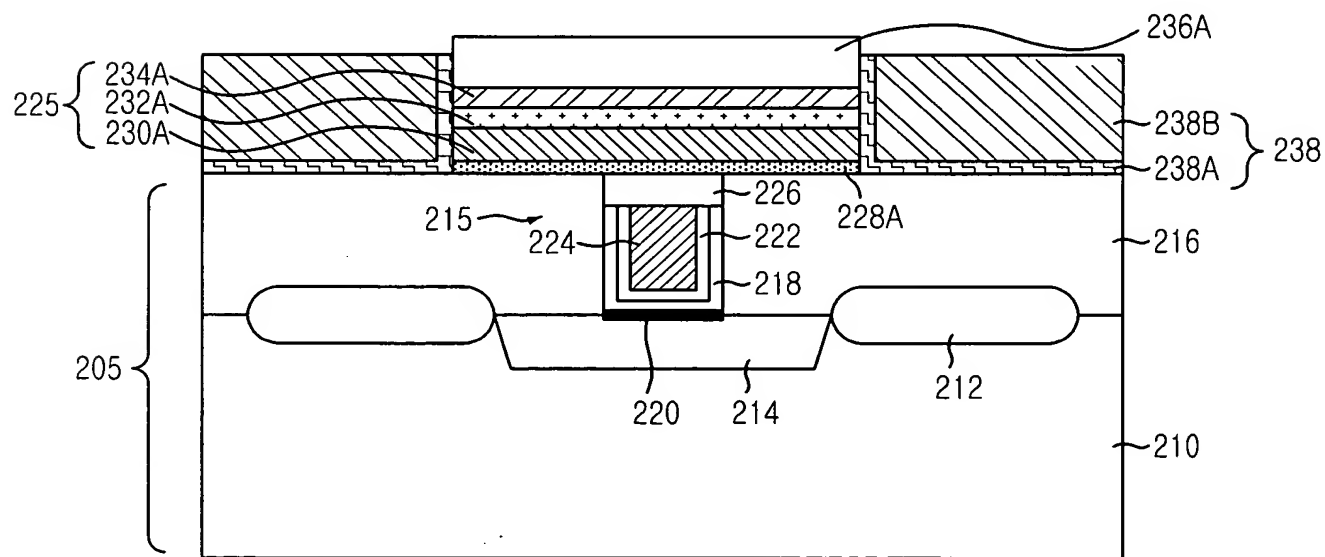


FIG. 5

